REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claim Rejections under 35 USC §103

Claims 1-2, 6, 8-9, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (U.S. Patent No. 6,747,977 BI) in view of Caves et al. (U.S. 6,788,691 B1). Applicants respectfully traverse these rejections.

Regarding claim 1, the Examiner has cited figure 1 of Smith et al. Applicants respectfully point to the Examiner that a careful reading of cited sections reveals that the system shown and described in figure 1 of Smith et al. has no relevance to what is recited in claims 1, 8, and 16.

Claim 1 recites "a first direct memory access unit configured to fetch a voice packet from said DSP sub-system, wherein said voice packet includes a physical phone line identifier". Rejecting this limitation, the Examiner stated that Smith et al. discloses "[a] first **memory access unit** (buffer 17), see figure 1, **configured to fetch** a voice packet **from DSP sub-system** (CODEC 14) system **for transmitting** packetized data received from a digital signal processor (DSP sub-system (Processor 21)" (Emphasis added). Applicants respectfully point to the Examiner that the buffer 17 is a "buffer" and not a direct memory access unit. Further, nowhere in the cited reference Smith et al. describe buffer 17 as configured to **fetch** a voice packet from the CODEC 14. In contrast, Smith et al. states that the CODEC data is stored in the buffer 17 (col. 8, lines 15-17). Further, the Examiner has stated that the buffer 17 is configured to transmit packetized data **received from a digital signal processor** (processor 21). In fact, actually Smith et al. states that the processor 21 is arranged to "interrogate information incident to the buffer 17." (col. 8, lines 22-24). Furthermore, nowhere in the cited sections Smith et al. teach physical phone line identifier as recited in claim 1. In

contrast, Smith et al. refers to channel, which includes multiplexed data. Therefore, Smith et al. does not teach a direct memory access unit as recited in claim 1.

As to the second direct memory access unit configured to fetch a signaling and management packet from said host processor, wherein said signaling and management packet includes a transmit channel identifier as recited in claim 1, the Examiner has stated that Smith et al. teaches:

> "A second **direct memory access unit** (channel buffer 25), see figure 1, **configured to fetch** for receiving a packet fetched from host processor (signal processor 19, figure 1) (see col. 6, lines 13-27, receiving the intermediate packet t be received at the broadband signal processor should be temporary stored or converted into a broadband packet for onward transmission; and generating a broadband packet including a header containing a length indication if the at least one intermediate packet is to be converted into a broadband packet for substantially instantaneous onward transmission, else temporary storing the at least one intermediate packet and incrementing a record of a number intermediate packets temporary stored in relation to said channel)." (Emphasis added).

First, the above description has no relevance to the second direct memory access unit recited in claim 1. Second, the channel buffer is again just that "a buffer". Third, the channel buffer is not configured to fetch anything, in fact, it is the signal processor 19, which is configured to buffer intermediate packets in the channel buffer 25 (*see* col. 9, lines 2-4). Fourth, the Examiner has cited Caves et al. as disclosing signaling and management packet from host processor and stated that

> "it would have been obvious to one skill in the art at the time of the invention to modify the system of Smith with the teaching of Caves to provide a signaling and management packet from host processor, wherein signaling and management packet includes a transmit channel identifier in order to interleave the voice, and signaling and management into the AAL2 data stream." (Emphasis added)

Applicants respectfully point to the Examiner that first, the reason the channel buffer is provided in Smith et al. is to temporarily store packets from a channel when the

channel supplies a relatively low number of intermediate packets until enough packets are accumulated in the temporary storage to warrant the construction of a broadband packet (*see* col. 8, line 66 – col. 9, line 29). Second, actually it is the signal processor 19 that stores these packets and the buffer 25 does not fetch packets from the processor 19 as the Examiner has asserted. Thus, not only Smith et al. does not teach limitation of claim 1 but in fact, cited sections have no relevance to limitations of claim 1.

Accordingly, the combination of cited references does not teach limitation of claims 1, 8, and 16 and these claims and those depend therefrom are patentably distinguishable from the combination of cited references.

As to claim 6, the Examiner has stated that

> Smith discloses first direct memory access unit (buffer 17) further operably configured to **fetch** voice packet from **a voice buffer associated with each digital signal processor** in DSP sub-system (CODEC 14) (see figure 1, (see col. 5, lines 56-62, the processor further comprising: means to packetise information from the narrowband domain into a slot selectively allocated to a call fro transmission to a slot selectively allocated to a call for transmission to an address unit, the packetized information containing a truncated header of reduced length arising from the slot allocated to the call inherently identifying the packet length thereof and the channel). (Emphasis added)

Applicants respectfully request a careful reading of claim 6. Claim 6 refers to the functionality of the first direct memory access unit. The Examiner has cited buffer 17 as the first direct memory access unit. Nowhere in the cited sections Smith et al. states that buffer 17 is configured to fetch from a voice buffer in fact, Smith et al. does not even discuss voice buffers associated with CODEC 14 and figure 1 (cited by the Examiner) does not show any voice buffer associated with each digital signal processor. Accordingly, Smith et al. does not teach this limitation.

Double Patenting

Claims 1, 16, 8 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,961,340 B2 in

view of Caves et at. (U.S. 6,788,691 B1). Applicants respectfully traverse these rejections.

A careful reading of cited sections of Caves et al. reveals that it actually refers to channel identifications (CID). The status record 412 stores CIDs of channels included in a virtual channel connection (VCC) and information about their activity status. On the other hand, a careful reading of claim 1 of the cited patent reveals that claim 1 already refers to CIDs. The first direct memory access unit forwards data stored in buffers corresponding to CIDs and the second direct memory access unit forwards stored data in response to CID and user-to-user identification filtering. Thus, both references refer to the same entity and there is no reason to combine them. Even if the teachings are combined, then they still do not result in anything new. Both references describe CIDs. Accordingly, claims 1, 8, and 16 are patentably distinguishable from the combination of cited references.

Applicant believes this application and the claims herein to be in a condition for allowance. Please charge any additional fees, or credit overpayment to Deposit Account No. 20-0668. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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